UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/204,479	12/03/1998	MARC TREMBLAY	004-3289	5561

22120 7590 03/08/2004

ZAGORIN O'BRIEN & GRAHAM, L.L.P.
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
ENG, DAVID Y	

ART UNIT	PAPER NUMBER
2155	33

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 33

Application Number: 09/204,479
Filing Date: December 03, 1998
Appellant(s): TREMBLAY ET AL.

Edward J. Marshall
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 20, 2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

No amendment after final has been filed.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

All claims stand or fall together.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,826,096	Baxter	10-1998
4,300,195	Raghunathan et al.	11-1981

Andrew S. Tanenbaum, "Structured Computer Organization", Prentice-Hall, 1976, pages 75-87.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3-6, 8-17, 19-21 and 23-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter (USP 5,826,095) in view of Tanenbaum (text book).

Attention of the Board is respectfully directed to Figure 2 of Baxter. With respect to claims 1, 3, 5-7, 17 and 19-23, Baxter taught a processor comprising:

A register file (260 in Baxter) divided into a plurality of registers,

A plurality of functional units (270) each associated with a register segment, and

A decoder (140) coupled to the register file and the functional units for explicitly deriving register specifiers (pointers) for addressing (pointing to) registers of the register file for retrieving operands therefrom so that arithmetic operations can be applied to the operands.

Baxter does not show how register specifier (the address of register in register file) is developed. Attention of the Board is respectfully directed to format 1 in Figure 3-19, section 3.3 (Addressing), section 3.3.2 (Direct Addressing), section 3.3.3. (Register

Addressing) and section 3.3.5. (Indexing) on pages 79-85 in Tanenbaum. Figure 3-19 shows an instruction having a format of four fields. The first field is the op-code. The rest of the three fields represent the operands upon which the op-code is operated. If the op-code is an add operation, the add instruction means to add the two operands represented by the last two fields and to store the result in the register represented by the second field (page 80). The other sections in Tanenbaum teach different methods that a register specifier can be formulated for accessing the operands from registers in a register file. One of the methods is auto-indexing (section 3.3.5, page 84 in Tanenbaum) wherein a one or a constant is automatically added to the previous address such that consecutively stored operands can be retrieved and operated upon by the op-code. If the operands of Baxter are consecutively stored, it would have been obvious to a person of ordinary skill in the art to use auto-indexing such that consecutively stored operands can be retrieved and acted upon by the op-codes. Other claims merely applied the same auto-indexing feature to instructions of different op-codes.

With respect to claim 4, see register file segment in Figure 2 of Baxter. VLIW processor is well known in the art (see Architectural and Implementation of a VLIW Supercomputer in "Other Publication" in Baxter). Further, Baxter has a plurality of functional units.

With respect to claims 8-16, see double precision floating point operation in lines 23-24 of column 4 of Baxter.

Claim 7 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter (USP 5,826,095) and Tanenbaum (text book) further in view of Raguunathan (USP 4,300,195).

Baxter and Tanenbaum teach claim combination set forth above. Call and Return Call instructions are well known in the art. See lines 26-31 of column 3 in Raghunathan. Raghunathan teaches transferring of control to a subroutine for handling the call interrupt in response to a call instruction. Raghunathan further teaches a pointer for pointing to the return address for returning control back to the interrupted program. It would have been obvious to a person of ordinary in the art to implement the Call and Return Call operations in Baxter such that control can be returned after interrupt.

(11) Response to Argument

With respect to the arguments at the top of page 4, the Examiner agrees with Appellants that auto-indexing of instructions (increments program counter automatically for accessing sequentially stored instructions) is well known in the art. Appellant's invention is to applied the same technique of auto-indexing of instructions stored in main memory to operands stored in register file. As explained in the rejections above, Tanenbaum is about auto-indexing of registers in register file which is exactly Appellants' invention. Appellants contended that the PTO has discounted important aspect of Appellants' claimed invention, namely, auto-indexing on operand registers. It appears that Appellants simply ignore Tanenbaum's teaching.

From the bottom of page 4 to the top of page 6, Appellants merely set forth the legal ground of their arguments. There is no merit argument presented in those pages. There is no specific argument presented as to why the rejections did not meet the standard.

Appellants' only arguments appeared on page 6 and portion of page 7. Appellants' sole argument appears to be that Tanenbaum teaches auto-indexing of instructions whereas Appellants' claimed invention is auto-indexing of operands. As admitted by Appellants, auto-indexing of instructions is well known in the art. Appellants' invention is to applied the same auto-indexing technique of instruction to operands. This is exactly Tanenbaum's teaching. In the last paragraph of Section 3.3 (lower bottom of page 80, Tanebaum wrote:

> "Up to this point we have paid relatively little attention to how the bits of an address field are interpreted to find the **operand**. One possibility is that they contain the memory address of the operand. There are, however, other possibilities as well, and in the following sections we will explore some of them."

As can be seen, Section 3.3.5 in Tanenbaum is about auto-indexing of operands and not instructions as argued by Appellants. See also the last paragraph of page 84. The section clearly is directed to operand addressing.

For the above reasons, it is believed that the rejections remain intact. It is therefore respectfully requested that the rejections be sustained.

Respectfully submitted,

David Y. Eng

DAVID Y. ENG
PRIMARY EXAMINER

ERIC COLEMAN
PRIMARY EXAMINER

March 3, 2004

Conferees
Eric Coleman
Le Luu

LE HIEN LUU
PRIMARY EXAMINER

SKJERVEN MORRILL MACPHERSON LLP
25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110